(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 932 103 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.07.1999 Bulletin 1999/30

(51) Int. Cl.[6]: **G06F 13/10**

(21) Application number: **98250026.6**

(22) Date of filing: **27.01.1998**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

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(54) Method and apparatus for transferring bi-directionally data between an IEEE 1394 bus and device

(57) The IEEE 1394 bus communication protocol has three layers: physical layer, link layer, and transaction layer. Typically, the transaction layer is realised by firmware whereas the other layers are implemented using chip sets. The link layer IC usually contains a FIFO having a capacity of e.g. 32k or 64k bits. Therefore, the link layer chip is the most costly part of a complete IEEE 1394 interface. Due to these cost reasons most ICs on the market are not bi-directional although the IEEE 1394 bus specification supports this feature. Incoming or outgoing data packets are intermediately stored in the FIFO. The current solution to this problem is to have two separate IEEE 1394 bus nodes assigned to the same application, the two nodes including two physical layer ICs and two link layer ICs. The inventors have found that although the physical link layer interface is not designed for this purpose, it works correctly with up to three link layer ICs and one physical layer IC if the additional link layer IC/ICs is/are programmed respectively. Therefore two or more link layer ICs can operate together with one physical layer IC in one node wherein the link layer ICs are connected to the same application or device.

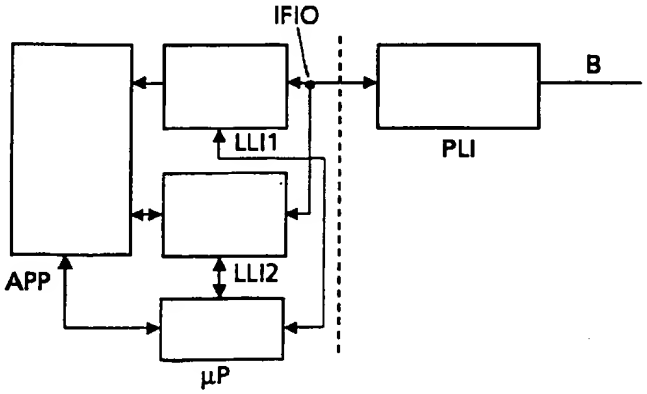

Fig.2

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Description

[0001] The present invention relates to a method and to an apparatus for transferring bi-directionally data between an IEEE 1394 bus and a device to be controlled by said bus.

Background

[0002] The IEEE 1394 bus is a low cost, high performance serial bus. It has a read/write memory architecture and a highly sophisticated communication protocol. Data rates of 100, 200 or 400Mbit/s can be transmitted in nearly real time. Simultaneously, data can be transmitted bi-directionally. The first ten bits of transmitted address values refer to one of up to 1023 possible IEEE 1394 bus clusters. The following six bits of the transmitted address values refer within a specific cluster to one of up to 63 nodes to which an application or device is assigned. Data between nodes can be exchanged without interaction of a host controller. Devices can be connected to or disrupted from the network at any time, allowing a plug and play behaviour. The standardised cable connection for the nodes has a length of 4.5m and contains three twisted cable pairs of which two pairs serve for data and control information transmission and the further pair carries supply voltages of 8V to 40V. Three level coding is used: HIGH (H), LOW (L), and HIGH IMPEDANCE (Z). H overrides L, L overrides Z. The characteristic impedance is 110Ω. There is also a version IEEE 1394-1995 of the bus specification including only two twisted pairs of cables on which no power supply voltage is present. The communication protocol has three layers: physical layer, link layer, and transaction layer. Typically, the transaction layer is realised by firmware whereas the other layers are implemented using chip sets.

[0003] The physical layer contains analog transceivers and a digital state machine. It handles bus auto-configuration and hot plug. It reclocks, regenerates and repeats all packets and forwards all packets to the local link layer. It carries out-packet framing, for example speed code, prefix, and packet end assembling. It arbitrates and transmits packets from the local link layer. Available IC types are e.g. TSB11C01, TSB11LV01, TSB21LV03, and TSB41LV03 of Texas Instruments, MB86611 of Fujitsu, and 21S750 of IBM.

[0004] The link layer performs all digital logic. It recognizes packets addressed to the node by address recognition and decodes the packet headers. It delivers packets to higher layers and generates packets from higher layers. It works either isochronous for AV data use or asynchronous for control data use.

[0005] In the isochronous mode a channel having a guaranteed bandwidth is established. There is a defined latency. The transmission is performed in 125µs time slots or cycles. Headers and data blocks of a packet have separate CRCs (cyclic redundancy check). This mode has a higher priority than the asynchronous data transfer mode.

[0006] The asynchronous mode is not time critical, but safe. It operates as an acknowledged service with a busy and retry protocol. Fixed addresses are used. Transmission takes place when the bus is idle. The asynchronous mode handles read request/response, write request/response, and lock request/response. It performs cycle control, CRC generation and validation. Available link layer IC types are e.g. TSB12C01A, TSB12LV21, TSB12LV31, and TSB12LV41 of Texas Instruments, and PDI1394L11 of Philips.

[0007] The transaction layer implements asynchronous bus transactions:

Read request/read response
Write request/write response
Lock request/lock response

As mentioned above it can be implemented by software running on a microcontroller, such as e.g. the i960 of SparcLite.

[0008] There may also be an AV (audio video) layer carrying out device control, connection management, timestamping, and packetising.

Invention

[0009] The link layer IC usually contains a FIFO (first in first out) memory having a capacity of e.g. 32k or 64k bits and further buffers and adapts the data coming from the application to the requirements of the IEEE 1394 bus specification. Therefore, the link layer chip contains a lot of circuitry and is the most costly part of a complete IEEE 1394 interface. Due to these cost reasons most ICs on the market are not bi-directional although the IEEE 1394 bus specification supports this feature. Incoming or outgoing data packets are intermediately stored in the FIFO.

It is true that some link layer ICs are bi-directional, but for a lot of applications, e.g. video data operation, the memory size of such standard bi-directional link ICs is sufficient only for either transmission or reception of isochronous data at any one time. Therefore, in practice, such ICs can only be used in one direction, i.e. real-time bidirectional data transfer is not possible. A larger memory size was not chosen for such standard link ICs, because no necessity for real-time bi-directional data transfer was seen which would justify the additional costs.

[0010] The current solution to this problem is to have two separate IEEE 1394 bus nodes assigned to the same application, the two nodes including two physical layer ICs, two link layer ICs, two microcontrollers, and an additional cable connection, i.e. a quite complicated and expensive solution. The physical separation of the two nodes adds to the network latency and requires an additional cable hop. Because only 16 cable hops are

allowed in the IEEE 1394 bus specification the latter requirement can cause a significant drawback in some applications.

[0011] It is one object of the invention to disclose a method for combining widely available, and therefore cheap, unidirectional IEEE 1394 bus link layer ICs to form a bidirectional data transfer functionality for an IEEE 1394 bus interface representing only one IEEE 1394 bus node. This object is achieved by the method disclosed in claim 1 or 2.

[0012] It is a further object of the invention to disclose an apparatus which utilises the inventive method. This object is achieved by the apparatuses disclosed in claims 5 and 6.

[0013] The inventors have found, confirmed by simulations, that although the physical link layer interface is not designed for this purpose, it works correctly with up to three link layer ICs and one physical layer IC if the additional link layer IC/ICs is/are programmed respectively.

According to the invention, two or more link layer ICs operate together with one physical layer IC in one node wherein the link layer ICs are connected to the same application or device. Advantageously, all link layer ICs, the physical layer IC and the application can be controlled by a single microcontroller performing e.g. software control and bus management. Link ICs can be selectively addressed using e.g. a unique I2C bus address or host chip enable.

[0014] The invention allows simultaneous real-time input and output of data packets or simultaneous input of two data packets, e.g. the reception of a video channel and an audio channel or the reception of two video channels, for instance for PIP (picture-in-picture) purposes.

[0015] In principle, the inventive method is suited for transferring bi-directionally data between an IEEE 1394 bus and a device to be controlled by said bus, wherein for interfacing between the bus and said device a physical layer IC and a first link layer IC is used and wherein a second link layer IC is also in operation which is connected on one side to the interface input/output of said first link layer IC and on the other side to said device,
wherein said first link layer IC performs input and output of bus-related data and said second link layer IC performs either input or output of bus-related data
or
wherein said first link layer IC performs input of first bus-related data and said second link layer IC performs input of second bus-related data and wherein said first and second bus-related data belong to different data streams, in particular two video data streams or one video and one audio data stream.

[0016] Advantageous additional embodiments of the inventive method are disclosed in the respective dependent claims.

[0017] In principle the inventive apparatus is suited for transferring bi-directionally data between an IEEE 1394 bus and a device to be controlled by said bus, and includes:

- a physical layer IC and a first link layer IC for interfacing between the bus and said device;
- a second link layer IC which is connected on one side to the interface input/output of said first link layer IC and
  on the other side to said device, wherein said first link layer IC performs input and output of bus-related data and said second link layer IC performs either input or output of bus-related data,
  or
  wherein said first link layer IC performs input of first bus-related data and said second link layer IC performs input of second bus-related data and said first and second bus-related data belong to different data streams, in particular two video data streams or one video and one audio data stream.

[0018] Advantageous additional embodiments of the inventive apparatus are disclosed in the respective dependent claim.

Drawings

[0019] Embodiments of the invention are described with reference to the accompanying drawings, which show in:

- Fig. 1 known IEEE 1394 double-node for bi-directional real-time video applications;
- Fig. 2 IEEE 1394 node for bi-directional real-time video applications according to the invention;
- Fig. 3 the IEEE 1394 node of Fig. 2 in more detail, including a capacitive isolation barrier;
- Fig. 4 an IEEE 1394 bus-connected set-top box, VCR and DVD player;
- Fig. 5 IEEE 1394 node for bi-directional real-time video applications according to a further embodiment of the invention.

Embodiments

[0020] In Fig. 1 a first physical layer IC PLI1 is connected via an IEEE 1394 bus cable connection to a second physical layer IC PLI2 which itself is also connected to the further IEEE 1394 bus cable B. PLI1 is at the other side assigned to a first link layer IC LLI1 for data input, and PLI2 is assigned to a second link layer IC LLI2 for data output. LLI1 and LLI2 are both assigned to the same application device APP. LLI1 and PLI1 via LLI1 are controlled by a first microcontroller µP1. LLI2 and PLI2 via LLI2 are controlled by a second microcontroller µP2. Application device APP can be controlled by µP1 and µP2, or by one of them. In both cases µP1 and µP2 may interact with each other (not depicted).

[0021] In Fig. 2 a single physical layer IC PLI is con-

nected to the IEEE 1394 bus cable B. PLI is at the other side assigned to a first link layer IC LLI1 for e.g. data input and to a second link layer IC LLI2 for data output and e.g. additionally data input. LLI1 and LLI2 are both assigned to the same application device APP. Advantageously, LLI1, LLI2, PLI via LLI1 or LLI2, and APP can all be controlled by a single mi

[0022] crocontroller µP. One more detailed configuration where the inventive bidirectional mode can be used, would be as in Fig. 3, where the first link IC LLI1 supports both input and output modes, and the second link IC LLI2 supports input (from the IEEE 1394 bus) only. This would be the simplest type of configuration for a bidirectional behaviour with multiple link layer ICs and one physical layer IC PLI. Fig. 3 depicts the main circuitry in PLI and LLI1/LLI2 for data exchange. Advantageously the components behind the dashed lines in LLI2 can be omitted or not used.

With the setup as in Fig. 3, only LLI1 would be able to be the cycle master on the bus. This means that cycle start packets would be sent directly from LLI1 to LLI2 via interface input/output IFIO and pad to pad connection PTPC. A simplification for LLI2 would be that the IEEE 1394-standardised link request pin LREQ (not depicted) to request the bus for transmission would not be required, as this IC is input only.

As mentioned above, simulations have shown that the capacitive isolation barrier feature of IEEE 1394 functions correctly with up to three link layer ICs and one physical layer IC. This isolation barrier is explained in detail in US-A-5 384 808 and uses the following component values:

Between physical power PPO and physical ground PGND a chain of two 5kΩ resistors R6 and R7 is arranged. Between link power LPO and link ground LGNDa chain of two 5kΩ resistors R1 and R2 is arranged. PLI is connected to the R6/R7 junction and LLI1/LLI2 are connected to the R1/R2 junction. Between the R1/R2 junction and the R6/R7 junction a chain of C1/1nF, R3/100Ω, R5/100Ω, and C2/1nF is inserted. From the R3/R5 junction a resistor R4/300Ω is connected to PGND.

Other versions of this PLI/LLI connecting circuitry are possible.

In this isolation barrier no appreciable degradation of logic levels occurs with the capacitive load of one or two extra link layer ICs on the pads of link A.

An additional addressing of each link layer IC can be achieved by a minor addition to a standard link layer IC design. An extra channel number register and comparator are required per extra link layer IC used, so that data streams can be addressed to a particular link layer IC.

Other configurations can also be used, for example two link layer ICs and one physical layer IC with both link layer ICs having input and output functionality.

[0023] The invention can e.g. be used for an application as depicted in Fig. 4: A set-top box STB with receiving unit RU, MPEG decoder MDEC and IEEE 1394 interface 1394S receives a digital TV program via satellite or cable. The receiving unit output signal is transmitted via IEEE 1394 bus for the purpose of recording to a video recorder VCRR including also a IEEE 1394 interface 1394V. Simultaneously, a DVD player DVDP replays a DVD disc and the DVD data is also transported via an IEEE 1394 bus interface 1394D to the IEEE 1394 bus interface 1394S of the set-top box in order to be decoded by the MPEG decoder MDEC and to be displayed on the screen of a television receiver TV. TV may still have an analog signal connection to the set-top box, but may also be connected to STB by an IEEE 1394 bus interface. So, the set-top box IEEE 1394 bus node 1394S needs a bi-directional functionality.

[0024] The further embodiment of Fig. 5 shows the connection of a single physical layer IC PLI to a slightly modified first link layer IC LLI1 for data output and e.g. additionally data input, and to a correspondingly modified second link layer IC LLI2 for data input, i.e. receive mode. LLI1 and LLI2 each include five registers REG1 to REG5 and a multiplexer or switch MUX which is controlled by a signal SW which determines whether the specific IC operates in the data receiving mode.

LLI1 and LLI2 have an additional contol signal input CTLIN and two additional outputs DOUT for data and CTLOUT for the contol signal. Bus control signal CTL passes through registers REG2 and REG4 and output CTLOUT of LLI1 to CTLIN of LLI2. Then it passes REG5 and MUX and is thereafter available within LLI2 as internal control signal CTL_INT. From the output of REG2 of LLI1 it is also fed to MUX and is thereafter available within LLI1 as internal control signal CTL_INT. Bus data signal D passes via input DIN through registers REG1 and REG3 and output DOUT of LLI1 to DIN of LLI2. At the output of REG1 of LLI1 and LLI2 the internal bus data signal D_INT is available within LLI1 and within LLI2.

The bus link request signal LREQ is coming from LLI1 only. Bus clock SCLK is distributed to both, LLI1 and LLI2. D, CTL, LREQ, and SCLK can be transferred between PLI and LLI1 via an isolation circuitry IS.

[0025] LLI1 and LLI2 are both assigned to the same application device.

Claims

1. Method for transferring bi-directionally data between an IEEE 1394 bus (B) and a device (APP) to be controlled by said bus, wherein for interfacing between the bus and said device a physical layer IC (PLI1, PLI) and a first link layer IC (LLI1) is used, **characterised** in that a second link layer IC (LLI2) is also in operation which is connected on one side to the interface input/output (IFIO) of said first link layer IC and on the other side to said device, wherein said first link layer IC performs input and output of bus-related data and said second link layer IC performs either input or output of bus-

related data.

2. Method for transferring bi-directionally data between an IEEE 1394 bus (B) and a device (APP) to be controlled by said bus, wherein for interfacing between the bus and said device a physical layer IC (PLI1, PLI) and a first link layer IC (LLI1) is used, **characterised** in that a second link layer IC (LLI2) is also in operation which is connected on one side to the interface input/output (IFIO) of said first link layer IC and on the other side to said device, wherein said first link layer IC performs input of first bus-related data and said second link layer IC performs input of second bus-related data and wherein said first and second bus-related data belong to different data streams, in particular two video data streams or one video and one audio data stream.

3. Method according to claim 1 or 2, wherein at least one further link layer IC is connected and operated in parallel with said second link layer IC.

4. Method according to any of claims 1 to 3, wherein said first and said second and/or said further link layer ICs are controlled by one microcontroller (μP).

5. Apparatus for transferring bi-directionally data between an IEEE 1394 bus (B) and a device (APP) to be controlled by said bus, including:

   - a physical layer IC (PLI1, PLI) and a first link layer IC (LLI1) for interfacing between the bus and said device;
   - a second link layer IC (LLI2) which is connected on one side to the interface input/output (IFIO) of said first link layer IC and on the other side to said device, wherein said first link layer IC performs input and output of bus-related data and said second link layer IC performs either input or output of bus-related data.

6. Apparatus for transferring bi-directionally data between an IEEE 1394 bus (B) and a device (APP) to be controlled by said bus, including:

   - a physical layer IC (PLI1, PLI) and a first link layer IC (LLI1) for interfacing between the bus and said device;
   - a second link layer IC (LLI2) which is connected on one side to the interface input/output (IFIO) of said first link layer IC and on the other side to said device, wherein said first link layer IC performs input of first bus-related data and said second link layer IC performs input of second bus-related data and wherein said first and second bus-related data belong to different data streams, in particular two video data streams or one video and one audio data stream.

7. Apparatus according to claim 5 or 6, wherein said first and said second link layer IC is controlled by one micro-controller (μP).

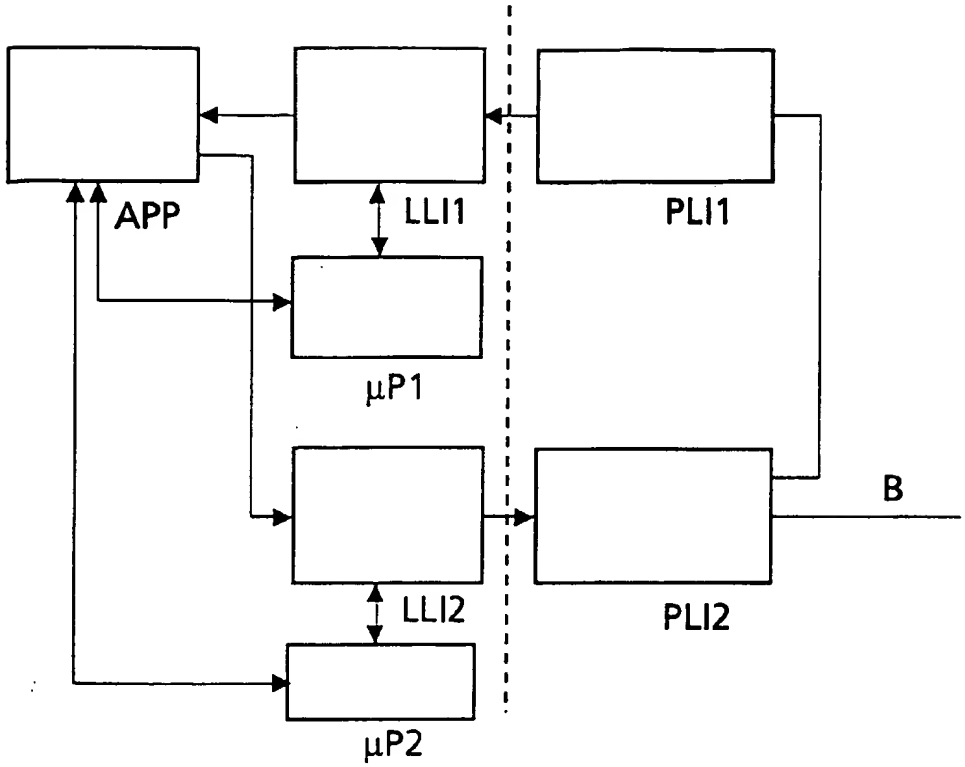

Fig.1

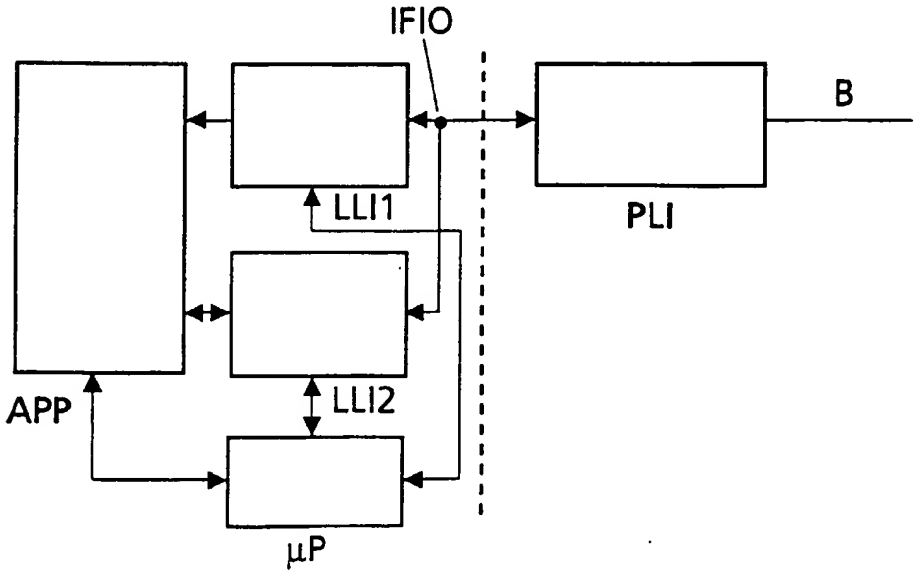

Fig.2

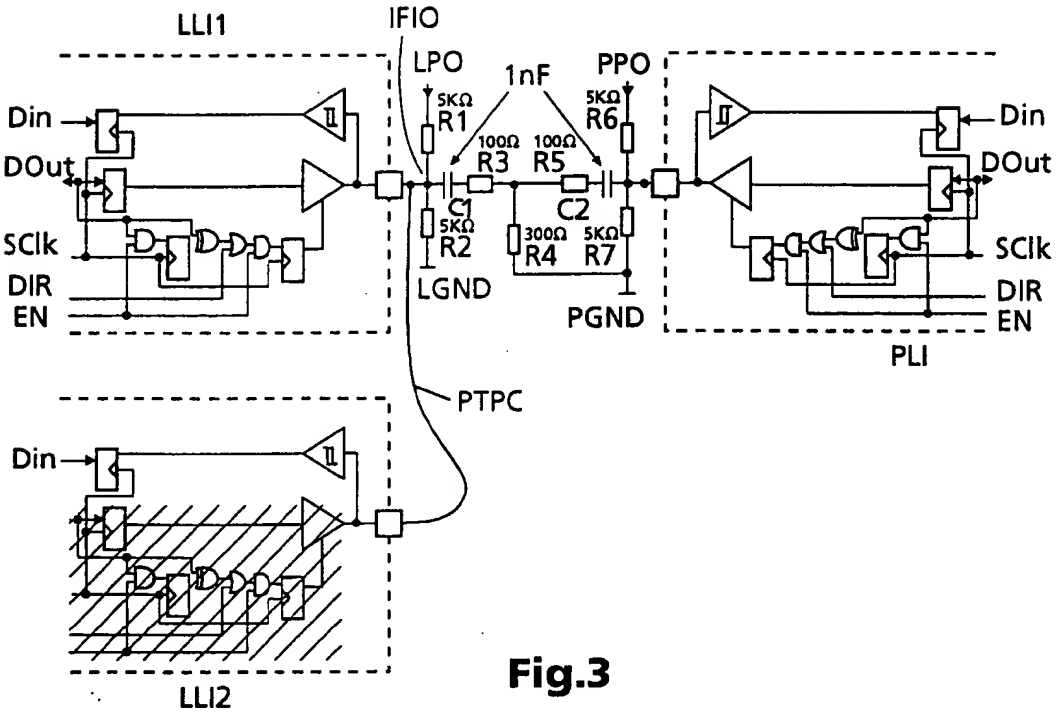

Fig.3

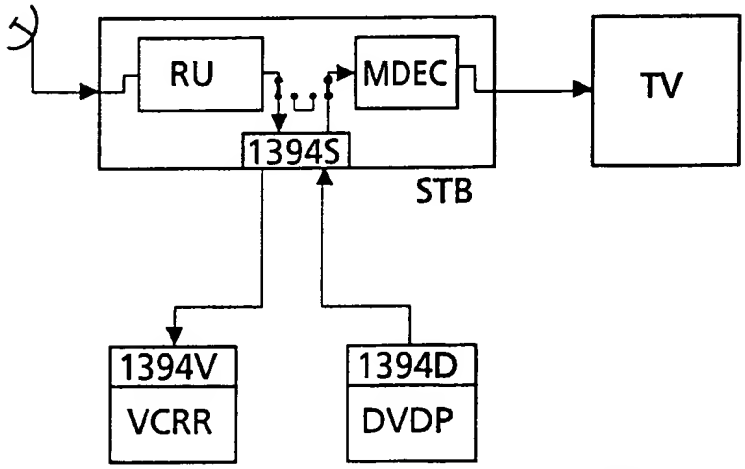

Fig.4

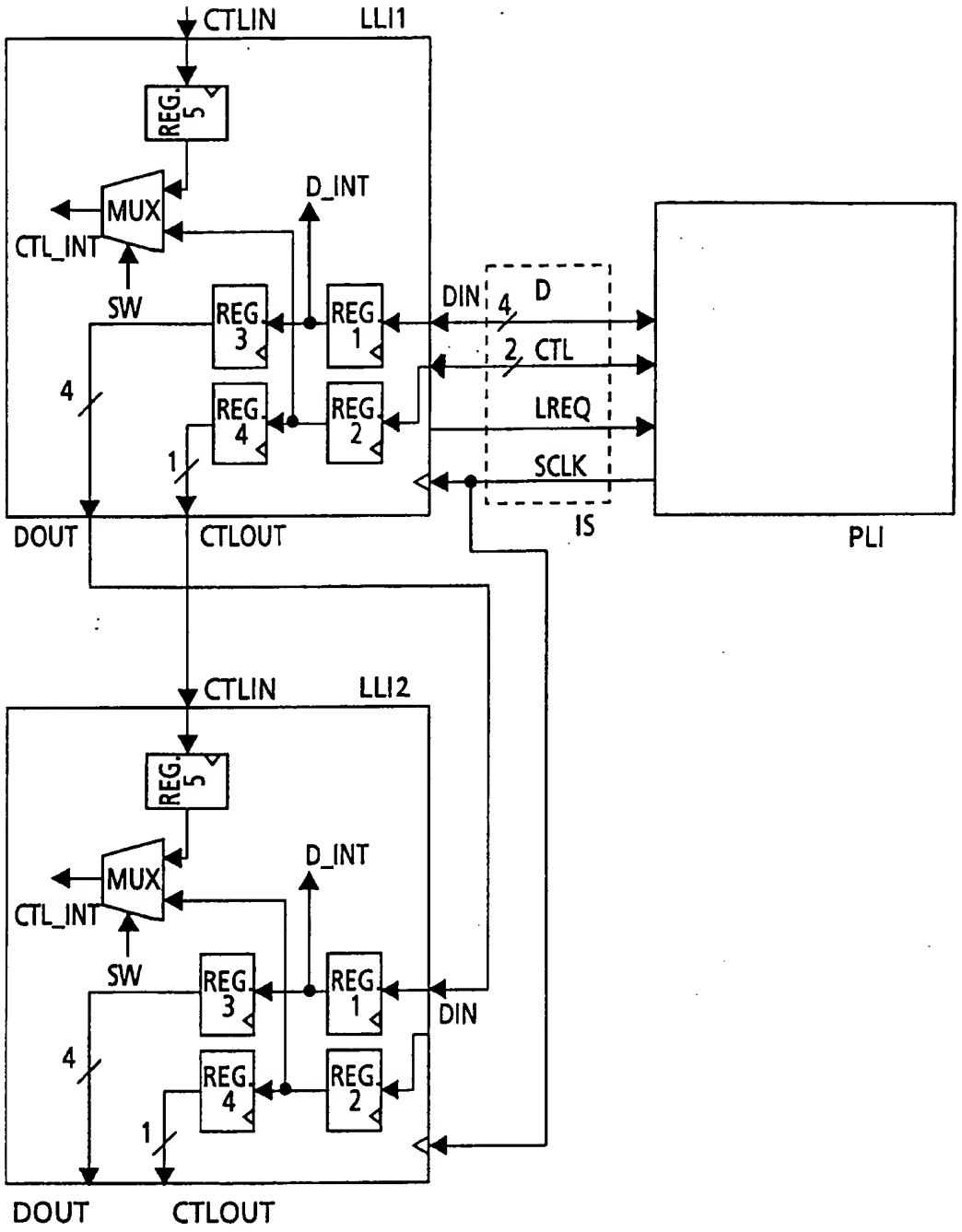

Fig.5

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EUROPEAN SEARCH REPORT

Application Number
EP 98 25 0026

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WO 97 28504 A (SONY ELECTRONICS INC ;SMYERS SCOTT D (US); FAIRMAN BRUCE (US)) 7 August 1997 * page 2, line 1 - line 29 * * page 8, line 19 - page 11, line 15 * * page 17, line 6 - page 18, line 24 * * abstract; claims 1-3; figures 1,4 *	1,2,5	G06F13/10
A	US 5 579 486 A (OPRESCU FLORIN ET AL) 26 November 1996 * column 1, line 28 - column 2, line 26 * * column 3, line 49 - column 4, line 14 * * column 5, line 60 - column 7, line 15 *	1-7	
A	EP 0 784 401 A (TOKYO SHIBAURA ELECTRIC CO) 16 July 1997 * column 7, line 15 - column 8, line 40 * * abstract; figure 5 *	1-7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 June 1998	NGUYEN XUAN HIEP C.

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